THAT WHICH IS CLAIMED IS:

1. A method for incrementing, decrementing or two's complementing a N bit string (K), comprising

generating an auxiliary string (M; $\overline{M}$) of N bits, in function of said string (K), whose least significant bit is independent from said string (K) and any other bit (M_I; $\overline{M_I}$), starting from the second least significant bit (M_1; $\overline{M_1}$) up to the most significant bit (M_{N-1}; $\overline{M_{N-1}}$), is a logic combination of a corresponding bit (K_{I-1}; $\overline{K_{I-1}}$) of said first string (K) or of a negated replica thereof ($\overline{K}$), starting from the least significant bit (K_0; $\overline{K_0}$) up to the second most significant bit (K_{N-2}; $\overline{K_{N-2}}$), and of the bits of said first string (K) or of the negated replica thereof ($\overline{K}$) less significant than said corresponding bit (K_0, ..., K_{I-2}; $\overline{K_0}$, ..., $\overline{K_{I-2}}$);

generating an output string (Y) as a logic combination of said auxiliary string (M; $\overline{M}$) and of said first string (K).

2. The method of claim 1, wherein the least significant bit of said auxiliary string (M) is always null and any other bit (M_I), starting from the second least significant bit (M_1) up to the most significant bit (M_{N-1}), is the logic OR of a corresponding bit of said first string (K_{I-1}) or of a negated replica thereof ($\overline{K_{I-1}}$) and of said bits less significant than said corresponding bit (K_0, ..., K_{I-2}; $\overline{K_0}$, ..., $\overline{K_{I-2}}$).

3. The method of claim 1, wherein

the least significant bit of said auxiliary string ($\overline{M}$) is always 1 and any other bit ($\overline{M_I}$), starting from the second least significant bit ($\overline{M_1}$) up to the most significant bit ($\overline{M_{N-1}}$), is the logic AND of a corresponding bit of said first string (K_{I-1}) or of a negated replica thereof ($\overline{K_{I-1}}$) and of said bits less significant than said corresponding bit (K_0, ..., K_{I-2}; $\overline{K_0}$, ..., $\overline{K_{I-2}}$).

4. The method of claim 1, further comprising generating an overflow flag (OF) as a logic combination among the most significant bits of said auxiliary string (M_{N-1}; $\overline{M_{N-1}}$) and of said first string (K_{N-1}).

5. The method of claim 2 for two's complementing said first string (K), wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said first string (K_{I-1});

said output string (Y) is obtained as XOR of said string (K) to be complemented and of said auxiliary string (M).

6. The method of claim 3 for two's complementing said first string (K), wherein

said other bit of the auxiliary string ($\overline{M_I}$) is obtained by ANDing the immediately less significant bit ($\overline{M_{I-1}}$) of said auxiliary string ($\overline{M}$) and a corresponding bit of said first string (K_{I-1});

said output string (Y) is obtained as negated XOR of said string (K) to be complemented and of said auxiliary string ($\overline{M}$).

7. The method of claim 2 for decrementing said first string (K), wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said first string (K_{I-1});

said output string (Y) is obtained as negated XOR of said first string (K) and of said auxiliary string (M).

8. The method of claim 3 for decrementing said first string (K), wherein

said other bit of the auxiliary string ($\overline{M_I}$) is obtained by ANDing the immediately less significant bit ($\overline{M_{I-1}}$) of said auxiliary string ($\overline{M}$) and a corresponding bit of said first string (K_{I-1});

said output string (Y) is obtained as XOR of said first string (K) and of said auxiliary string ($\overline{M}$).

9. The method of claim 2 for incrementing said first string (K), wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and the negated replica ($\overline{K_{I-1}}$) of a corresponding bit of said first string (K_{I-1});

said output string (Y) is obtained by XORing said auxiliary string (M) and a negated replica of said

first string (K).

10. The method of claim 3 for incrementing said first string (K), wherein

said other bit of the auxiliary string ($\overline{M_I}$) is obtained by ANDing the immediately less significant bit ($\overline{M_{I-1}}$) of said auxiliary string ($\overline{M}$) and a corresponding bit of said first string (K_{I-1});

said output string (Y) is obtained as negated XOR of said first string (K) and of said auxiliary string ($\overline{M}$).

11. The method of claims 2 and 4 for two's complementing or decrementing said first string (K), wherein said overflow flag (OF) is generated by ANDing the most significant bit of said first string (K_{N-1}) and a negated replica of the most significant bit of said auxiliary string (M_{N-1}).

12. The method of claims 3 and 4 for two's complementing or decrementing said first string (K), wherein said overflow flag (OF) is generated by ANDing the most significant bit of said first string (K_{N-1}) and the most significant bit of said auxiliary string ($\overline{M_{N-1}}$).

13. The method of claims 2 and 4 for incrementing said first string (K), wherein said overflow flag (OF) is generated by ANDing the negated replicas of the most significant bits of said first string (K_{N-1}) and of said auxiliary string (M_{N-1}).

14. The method of claims 3 and 4 for

incrementing said first string (K), wherein said overflow flag (OF) is generated by ANDing the negated replica of the most significant bit of said first string (K_{N-1}) and the most significant bit of said auxiliary string ($\overline{M_{N-1}}$).

15. The method of claim 11 for two's complementing said first string (K) with correction of the output in case of overflow, wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

the most significant bit of said output string (Y) is obtained by NORing the most significant bit of said first string (K_{N-1}) and the negated replica of the most significant bit of said auxiliary string (M_{N-1}),

any other bit of said output string (Y) is obtained by ORing the overflow flag (OF) and the logic XOR between corresponding bits of said first string (K) and of said auxiliary string (M).

16. The method of claim 11 for two's complementing said first string (K) with correction of the output in case of overflow, wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

the most significant bit of said output string (Y) is obtained by NORing the most significant bit of said first string (K_{N-1}) and the negated replica of the most significant bit of said auxiliary string

(M_{N-1}),

any other bit of said output string (Y) is obtained by XORing the overflow flag (OF) and the logic XOR between corresponding bits of said first string (K) and of said auxiliary string (M).

17. The method of claim 11 for decrementing said first string (K) with correction of the output in case of overflow, wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

the most significant bit of said output string (Y) is obtained by ORing the most significant bit of said first string (K_{N-1}) and the negated replica of the most significant bit of said auxiliary string (M_{N-1});

any other bit of said output string (Y) is obtained by XORing the negated replica of the overflow flag (OF) and the logic XOR between corresponding bits of said first string (K) and of said auxiliary string (M).

18. The method of claim 13 for incrementing said first string (K) with correction of the output in case of overflow, wherein

said other bit of the auxiliary string (M_I) is obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and the negated replica ($\overline{K_{I-1}}$) of a corresponding bit of said string (K_{I-1});

the most significant bit of said output string (Y) is obtained by NORing the most significant

bit of said first string (K_{N-1}) and the negated replica of the most significant bit of said auxiliary string (M_{N-1});

any other bit of said output string (Y) is obtained by ORing the overflow flag (OF) and the logic XOR between corresponding bits of said first string (K) and of said auxiliary string (M).

19. A circuit for incrementing, decrementing or two's complementing a N bit string (K), comprising

an auxiliary circuit (OR MASK; AND MASK) generating an auxiliary string (M; $\overline{M}$) of N bits, in function of said string (K), whose least significant bit is independent from said string (K) and any other bit (M_I; $\overline{M_I}$), starting from the second least significant bit (M_1; $\overline{M_1}$) up to the most significant bit (M_{N-1}; $\overline{M_{N-1}}$), is a logic combination of a corresponding bit (K_{I-1}; $\overline{K_{I-1}}$) of said first string (K) or of a negated replica thereof ($\overline{K}$), starting from the least significant bit (K_0; $\overline{K_0}$) up to the second most significant bit (K_{N-2}; $\overline{K_{N-2}}$), and of the bits of said first string (K) or of the negated replica thereof ($\overline{K}$) less significant than said corresponding bit (K_0, ..., K_{I-2}; $\overline{K_0}$, ..., $\overline{K_{I-2}}$);

logic circuit means generating an output string (Y) as a logic combination of said auxiliary string (M; $\overline{M}$) and of said first string (K).

20. The circuit of claim 19, wherein said auxiliary circuit (OR MASK) generates the auxiliary string (M) with the least significant bit always null,

the second least significant bit of said auxiliary string (M) as replica of the least significant bit of the first string (K_0) or as negated replica thereof ($\overline{K_0}$), and further comprises

N-2 OR gates each generating a respective bit of said auxiliary string (M), starting from the third least significant bit (M_2) up to the most significant bit (M_{N-1}) by ORing a corresponding bit (K_{I-1}; $\overline{K_{I-1}}$) of said first string (K) or of a negated replica thereof ($\overline{K}$), starting from the least significant bit (K_0; $\overline{K_0}$) up to the second most significant bit (K_{N-2}; $\overline{K_{N-2}}$), and the bits of said first string (K) or of the negated replica thereof ($\overline{K}$) less significant than said corresponding bit (K_0, ..., K_{I-2}; $\overline{K_0}$, ..., $\overline{K_{I-2}}$).

21. The circuit of claim 19, wherein said auxiliary circuit (OR MASK) generates the auxiliary string (M) with the least significant bit always null, the second least significant bit of said auxiliary string (M) as replica of the least significant bit of the first string (K_0) or as negated replica thereof ($\overline{K_0}$), and further comprises

N-2 OR gates each generating a respective bit of said auxiliary string (M), starting from the third least significant bit (M_2) up to the most significant bit (M_{N-1}), disposed in a cascade of pairs of logic gates, the gates of a first pair generating the third and fourth least significant bits of said auxiliary string (M_2, M_3) by ORing the two (K_0, K_1) and the three least significant bits (K_0, K_1, K_2), respectively, of said first string (K) or of the negated replica thereof ($\overline{K}$), each pair of OR gates being input with a

respective pair of consecutive bits first (K_{I-2}) and second (K_{I-1}) of said first string (K) or of the negated replica thereof ($\overline{K}$) and the most significant bit of said auxiliary string generated by the pair of gates that precedes in the cascade (M_{I-2}), and generating two consecutive bits of said auxiliary string (M_{I-1}, M_I) by ORing said most significant bit generated by the pair of gates that precedes in the cascade (M_{I-2}) and respectively said first bit (K_{I-2}) and both said bits first (K_{I-2}) and second (K_{I-1}) of said respective pair of bits.

22. The circuit of claim 19, wherein said auxiliary circuit (OR MASK) generates the auxiliary string (M) with the least significant bit always null, the second least significant bit of said auxiliary string (M) as replica of the least significant bit of the first string (K_0) or as negated replica thereof ($\overline{K_0}$), and further comprises

a cascade of N-2 OR gates input with a respective bit of said first string (K) or of the negated replica thereof in order starting from the second least significant bit (K_1) up to the second most significant bit (K_{N-2}), each gate generating a respective bit of said auxiliary string (M), starting from the third least significant bit (M_2) up to the most significant bit (M_{N-1}), as logic OR of the respective bit of said first string (K) or of the negated replica thereof and of the bit of the auxiliary string (M) generated by the OR gate that precedes in the cascade.

23. The circuit of claim 19, wherein said auxiliary circuit (AND MASK) generates the auxiliary

string ($\overline{M}$) with the least significant bit always equal to 1, the second least significant bit of said auxiliary string ($\overline{M}$) as replica of the least significant bit of the first string (K_0) or as negated replica thereof ($\overline{K_0}$), and further comprises

a cascade of N-2 AND gates input with a respective bit of said first string (K) or of the negated replica thereof in order starting from the second least significant bit (K_1) up to the second most significant bit (K_{N-2}), each gate generating a respective bit of said auxiliary string ($\overline{M}$), starting from the third least significant bit ($\overline{M_2}$) up to the most significant bit ($\overline{M_{N-1}}$), by ANDing the respective bit of said first string (K) or of a negated replica thereof and the bit of the auxiliary string ($\overline{M}$) generated by the AND gate that precedes in the cascade.

24. The circuit of claim 19, comprising an overflow control circuit (OVERFLOW CHECK) generating an overflow flag (OF) as logic combination among the most significant bits of said auxiliary string (M_{N-1}; $\overline{M_{N-1}}$) and of said first string (K_{N-1}).

25. The circuit of claim 22 for two's complementing said first string (K), wherein

each of said bits of the auxiliary string (M_I) starting from the third least significant bit (M_2) are obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

said logic circuit means comprise an array of XOR gates, generating bits of said output string (Y) by

XORing respective bits of said string to be complemented (K) and of said auxiliary string (M).

26. The circuit of claim 22 for decrementing said first string (K), wherein

each of said bits of the auxiliary string (M_I) starting from the third least significant bit (M_2) are obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

said logic circuit means comprise an array of XOR gates, generating bits of a two's complement string (Z) by XORing respective bits of said string to be complemented (K) and of said auxiliary string (M), and an array of NOT gates each input with a bit of the two's complement string and generating a corresponding bit of said output string (Y).

27. The circuit of claim 22 for incrementing said first string (K), wherein

each of said bits of the auxiliary string (M_I) starting from the third least significant bit (M_2) are obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and the negated replica ($\overline{K_{I-1}}$) of a corresponding bit of said string (K_{I-1});

said logic circuit means comprise an array of XOR gates, generating bits of said output string (Y) by XORing respective bits of said string to be complemented (K) and of said auxiliary string (M).

28. The circuit of claims 20 and 24 for two's complementing or decrementing said first string (K), wherein said overflow check circuit (OVERFLOW

CHECK) is a logic AND gate generating said overflow flag (OF), input with the most significant bit of said first string (K_{N-1}) and a negated replica of the most significant bit of said auxiliary string (M_{N-1}).

29. The circuit of claims 23 and 24 for two's complementing or decrementing said first string (K), wherein said overflow check circuit (OVERFLOW CHECK) is a logic AND gate generating said overflow flag (OF), input with the most significant bits of said first string (K_{N-1}) and of said auxiliary string ($\overline{M_{N-1}}$).

30. The circuit of claims 20 and 24 for incrementing said first string (K), wherein said overflow check circuit (OVERFLOW CHECK) is a logic AND gate generating said overflow flag (OF), input with the negated replicas of the most significant bits of said first string (K_{N-1}) and of said auxiliary string (M_{N-1}).

31. The circuit of claims 23 and 24 for incrementing said first string (K), wherein said overflow check circuit (OVERFLOW CHECK) is a logic AND gate generating said overflow flag (OF), input with a negated replica of the most significant bit of said first string (K_{N-1}) and the most significant bit of said auxiliary string ($\overline{M_{N-1}}$).

32. The circuit of claim 22 for incrementing or decrementing an input string (X) constituted by a number N of bits, comprising

an input terminal for receiving a command signal (ID) of the operation to be performed;

an array of N XOR gates each input with a respective bit of said input string (X) and with said

command signal (ID) generating a corresponding bit of said first string (K);

each of said bits of the auxiliary string (M_I) starting from the third least significant bit (M_2) are generated by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

said circuit logic means comprising an array of logic gates generating bits of said output string (Y) by XORing a negated replica of said selection command (ID) and the logic XOR of respective bits of said input string (X) and of said auxiliary string (M).

33. The circuit of claim 22, comprising

a logic selection circuit (SEL) input with command signals (ID, TC) identifying the operation to be performed and generating a pair of selection signals first (INV_OUT) and second (INV_IN) whose logic state depends on the operation to be carried out,

an array of N input XOR gates each input with a respective bit of said input string (X) and said second selection signal (INV_IN), generating said first bit string (K),

each of said bits of the auxiliary string (M_I) starting from the third least significant bit (M_2) are obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

said logic circuit means comprising an array of logic gates generating bits of said output string (Y) by XORing said first selection signal (INV_OUT) and the logic XOR of respective bits of said input string (X) and of said auxiliary string (M).

34. The circuit of claim 28 for two's complementing with correction of the output in case of overflow, wherein

each of said bits of the auxiliary string (M_I) starting from the third least significant bit (M_2) are obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and a corresponding bit of said string (K_{I-1});

said logic circuit means comprise

an OR gate input with the most significant bit of said first string (K_{N-1}) and the negated replica of the most significant bit of said auxiliary string (M_{N-1}), generating the most significant bit of a two's complement string to be corrected (Z_{N-1}),

an array of XOR gates generating the other bits of said two's complement string to be corrected (Z) by XORing corresponding bits of said first string (K) and of said auxiliary string (M); a correction circuit (CLIP) having

a NOT gate generating the most significant bit of said output string (Y_{N-1}) as negated replica of the most significant bit of said two's complement string to be corrected (Z_{N-1}),

an array of N-1 OR gates generating respective other bits of said output string (Y), each gate being input with said overflow flag (OF) and with an output of a respective gate XOR of said array.

35. The circuit of claim 28 for two's complementing or decrementing with correction of the output in case of overflow, having an input terminal receiving a selection signal (INV_OUT) of the operation to be performed, wherein

each of said bits of the auxiliary string (M_I)

starting from the third least significant bit (M_2) are obtained by ORing the immediately less significant bit (M_{I-1}) of said auxiliary string (M) and of a corresponding bit of said string (K_{I-1});

said logic circuit means comprise

an OR gate input with the most significant bit of said first string (K_{N-1}) and the negated replica of the most significant bit of said auxiliary string (M_{N-1}), generating the most significant bit of a two's complement string to be corrected (Z_{N-1}),

an array of XOR gates generating the other bits of said two's complement string to be corrected (Z) by XORing corresponding bits of said first string (K) and of said auxiliary string (M);

an output logic circuit input with said two's complement string (Z), said overflow flag (OF) and said selection signal and said selection signal (INV_OUT), generating an output bit string (Y) equal to said two's complement string (Z) or obtained by negating all the bits thereof depending on the logic state of said selection signal (INV_OUT) and of said overflow flag (OF).

36. The circuit of claim 35 for two's complementing or decrementing with correction of the output in case of overflow, wherein said output logic circuit comprises

a logic correction circuit (CLIP) generating a negated replica of said selection signal ($\overline{\text{INV\_OUT}}$) and a correction signal (INVCLIP) by XORing said selection signal (INV_OUT) and said overflow flag (OF);

an array of N logic XOR gates, one of them being input with the most significant bit (Z_{N-1}) of said two's complement bit string (Z) and with said negated

replica ($\overline{\text{INV\_OUT}}$) generating the most significant bit of the output string (Y_{N-1}), and each other XOR gate being input with a respective other bit of said two's complement string (Z) and said correction signal (INVCLIP) generating corresponding other bits of the output string (Y).

37. A multifunction circuit (DIT) for decrementing, incrementing or two's complementing an input N bit string (X), comprising

a logic selection circuit (SEL) input with command signals (ID, TC) identifying the operation to be performed and generating a pair of selection signals first (INV_OUT) and second (INV_IN) whose logic state depends on the operation to be performed,

an array of N XOR input gates each input with a respective bit of said input string (X) and with said first logic signal (INV_IN), generating said first bit string (K),

a circuit for two's complementing or decrementing as defined in claim 35, input with said first bit string (K) and generating said output bit string (Y).

38. The multifunction circuit (DIT) of claim 37, wherein said selection circuit (SEL) is input with a pair of command signals first (ID) and second (TC) and generates

said first logic signal (INV_OUT) by NORing said command signals (ID, TC);

said second logic signal (INV_IN) by ANDing said first command signal (ID) and a negated replica of said second command signal (TC).